WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip;

an alignment mark which is formed by part of an uppermost interconnection layer in a multilevel interconnection that is formed on the semiconductor chip and obtained by stacking low-permittivity insulating layers and interconnection layers, the alignment mark being arranged adjacent to each corner of the semiconductor chip; and

a conductive member which is buried in a contact hole formed in the low-permittivity insulating layer below the alignment mark, and contacts the alignment mark.

2. A device according to claim 1, wherein

the conductive member includes plugs which are buried in contact holes formed in the respective insulating layers in the multilevel interconnection, and

the alignment mark contacts a surface of the semiconductor chip via the plugs.

3. A device according to claim 1, which further comprises an element formed in the semiconductor chip, and

in which the alignment mark is electrically connected to the element.

4. A device according to claim 1, wherein

the conductive member is formed by part of an interconnection layer in the multilevel interconnection.

5. A device according to claim 1, further comprising a barrier film which is interposed between a low-permittivity insulating layer and an interconnection layer in the multilevel interconnection, and prevents oxidization and diffusion of the interconnection layer.

6. A device according to claim 5, wherein the barrier film includes an SiCN film.

7. A device according to claim 1, wherein the low-permittivity insulating layer has a relative dielectric constant of 3.0 to 2.5.

8. A device according to claim 1, wherein the alignment mark has a width of not less than 10 μm.

9. A semiconductor device comprising:

a semiconductor chip;

a guard ring which is formed by part of an uppermost interconnection layer in a multilevel interconnection that is formed on the semiconductor chip and obtained by stacking low-permittivity insulating layers and interconnection layers, the guard ring being arranged adjacent to each corner of the semiconductor chip; and

a conductive member which is buried in a contact hole formed in the low-permittivity insulating layer

below the guard ring, and contacts the guard ring.

10. A device according to claim 9, wherein the guard ring is arranged along four sides of the semiconductor chip.

11. A device according to claim 9, wherein

the conductive member includes plugs which are buried in contact holes formed in the respective insulating layers in the multilevel interconnection, and

the guard ring contacts a surface of the semiconductor chip via the plugs.

12. A device according to claim 9, wherein the conductive member is formed by part of an interconnection layer in the multilevel interconnection.

13. A device according to claim 9, further comprising a barrier film which is interposed between a low-permittivity insulating layer and an interconnection layer in the multilevel interconnection, and prevents oxidization and diffusion of the interconnection layer.

14. A device according to claim 13, wherein the barrier film includes an SiCN film.

15. A device according to claim 9, wherein the low-permittivity insulating layer has a relative dielectric constant of 3.0 to 2.5.

16. A device according to claim 9, wherein

the guard ring has a width of not less than 10 μm.

17. A semiconductor device comprising:

a semiconductor chip;

a guard ring which is formed by part of an uppermost interconnection layer in a multilevel interconnection that is formed on the semiconductor chip and obtained by stacking low-permittivity insulating layers and interconnection layers, the guard ring being arranged adjacent to each corner of the semiconductor chip;

a first conductive member which is buried in a first contact hole formed in the low-permittivity insulating layer below the guard ring, and contacts the guard ring;

an alignment mark which is formed by part of the uppermost interconnection layer in the multilevel interconnection, and arranged near at least one corner of the semiconductor chip; and

a second conductive member which is buried in a second contact hole formed in the low-permittivity insulating layer below the alignment mark, and contacts the alignment mark.

18. A device according to claim 17, wherein

the first conductive member includes first plugs which are buried in contact holes formed in the respective insulating layers in the multilevel interconnection, and

the guard ring contacts a surface of the semiconductor chip via the first plugs.

19. A device according to claim 17, wherein

the second conductive member includes second plugs which are buried in contact holes formed in the respective insulating layers in the multilevel interconnection, and

the alignment mark contacts a surface of the semiconductor chip via the second plugs.

20. A device according to claim 17, wherein the guard ring is arranged along four sides of the semiconductor chip.